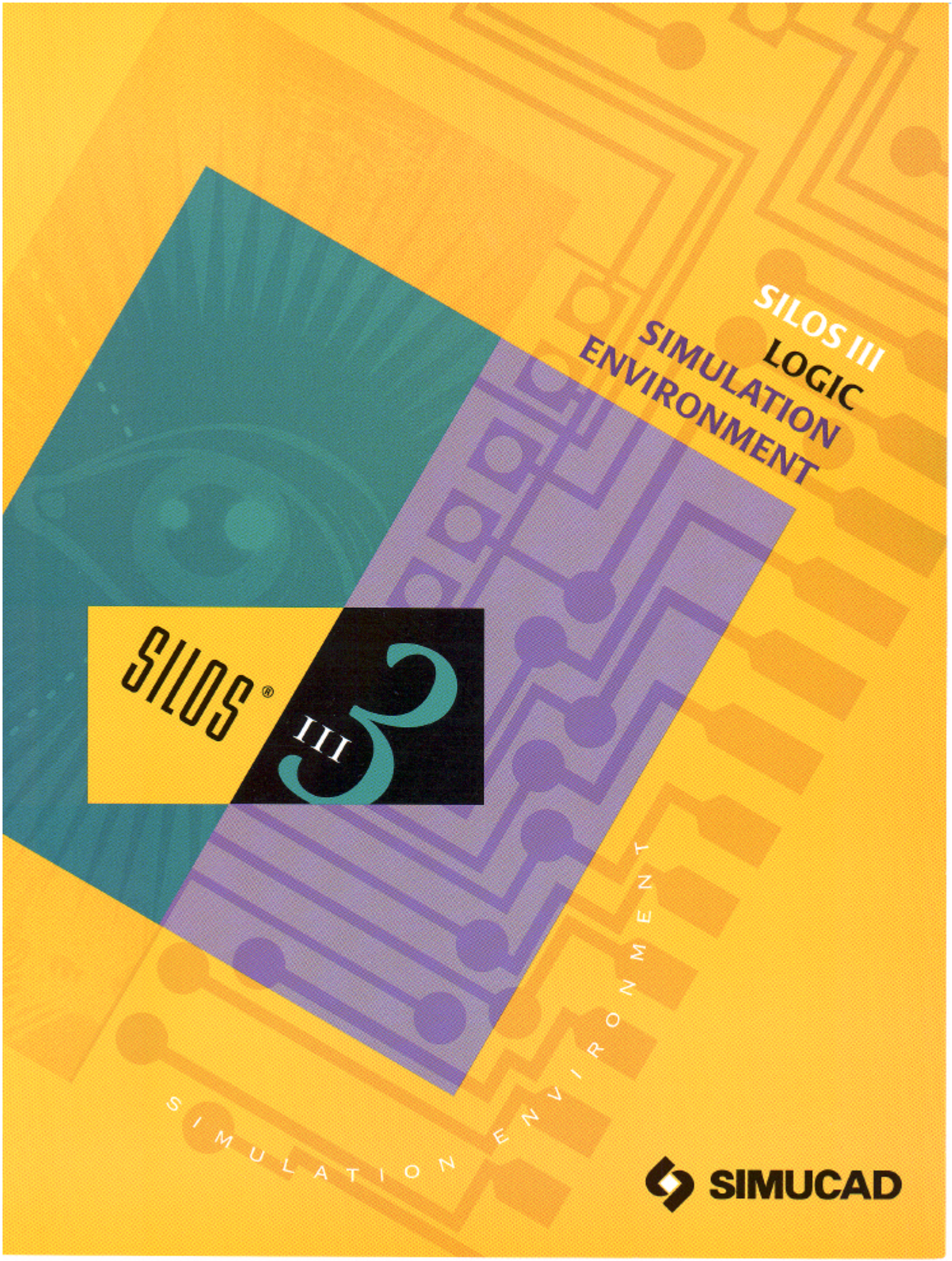

SILOS III
LOGIC
SIMULATION
ENVIRONMENT
SILOS®
III
SIMULATION ENVIRONMENT
SIMUCAD

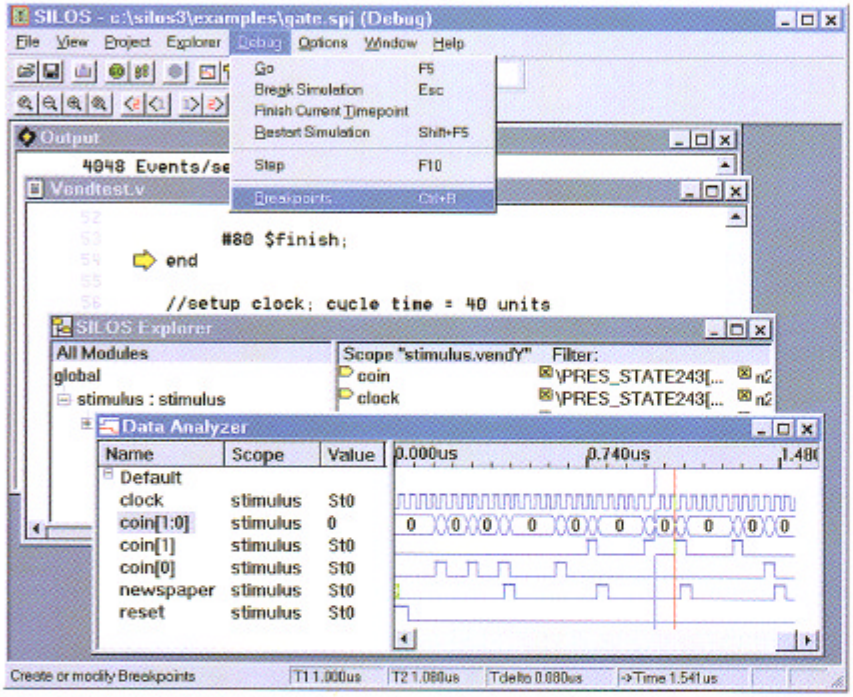
SILOS III's high performance logic simulation environment supports the Verilog Hardware Description Language for simulation at multiple levels of abstraction.

The Environment's state-of-the-art architecture incorporates an exclusive integrated / interactive multi-tasking graphical debugging environment that provides unsurpassed accuracy and outstanding performance.

Overview:

The SILOS III Simulation Environment is the next generation of Simucad's popular SILOS simulator which was first introduced in 1983. With more than 9,000 copies of SILOS in use today, it continues to be one of the most highly utilized simulators on the market. The integrated, interactive logic and fault simulation environment has evolved to meet the demanding needs of today's deep-submicron technologies.

SILOS III uses the Verilog Hardware Description Language to support a top-down design methodology. Its highly efficient simulation algorithms accommodate large hierarchical designs while utilizing limited amounts of system memory. The exclusive debugging environment merges the SILOS III Simulator, HDL Source Code Editor, Watch Window, Hierarchy Explorer, Two-dimensional Graphical Tracing utility and the Silos Data Analyzer waveform display into an interactive multi- tasking productivity tool. The debugging environment will dramatically reduce model development time and provide unparalleled designer productivity.



The Silos Simulation Environment has been specifically designed by designers for designers. The principle requirement was that it must provide the highest level of productivity to the digital designer developing and analyzing new models. To achieve this, Simucad's engineers have incorporated many performance enhancing features to improve simulation throughput speed in the debugging mode.

Comprehensive Feature Set:

- Interactive High Performance Logic Simulation
- Silos Data Analyzer™
- Two-Dimensional Graphical Signal Tracing Mode
- Silos Hierarchy Explorer
- HDL Source Code Editor
- Watch Window
- Productivity Enhancing Features:
  - Graphical User Interface
  - Advanced "Save All" Utility
  - Simulation Project Management
  - Highly Efficient Memory Utilization
- SILOS HyperFault™ Simulation System (Optional)

Easy to Learn and Use:

SILOS III was developed with the goal of creating a simulation environment that supports the industry standard hardware description language. The extensive availability of Verilog HDL-based ASIC and FPGA libraries and tools will minimize overall model development. Thorough syntax checking allows errors to be detected quickly while the integrated HDL source debugging utility and the two-dimensional gate level signal tracing utility are powerful tools to assist with new model development.

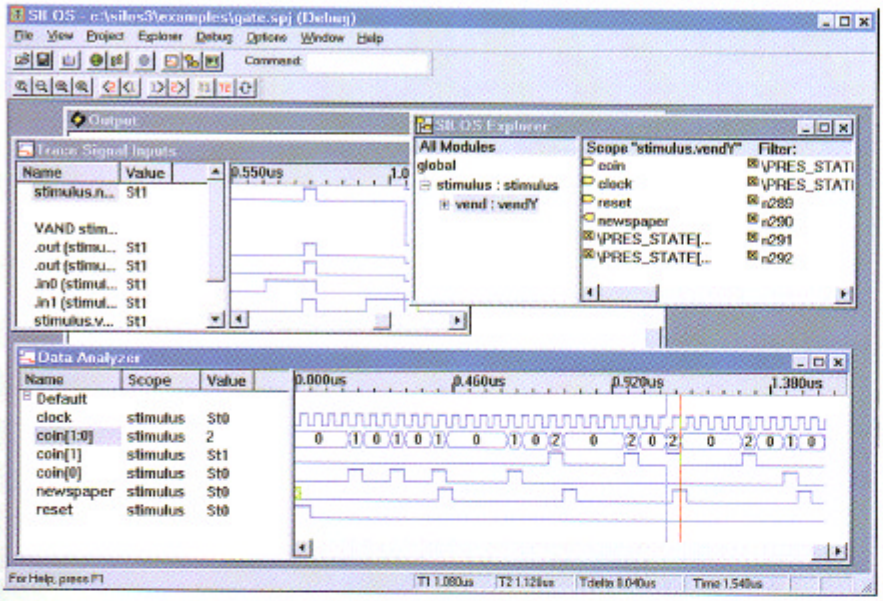
SILOS III uses only industry standard graphical user interfaces, including: Windows 95 and Windows NT for personal computers and X-Windows / MOTIF for UNIX workstations. The graphical user interface is identical in form and function regardless of the hardware platform or windowing system. The menu-oriented user interface allows the designer to intuitively control all aspects of the simulation environment without the need to memorize numerous abstract commands.

Powerful Save All Utilities:

SILOS III incorporates a sophisticated Save All utility that saves the netlist topology and all of the simulation results. This powerful feature allows you to save and review the results of the entire simulation database including every state and strength for all signals at every simulation time point, with almost no penalty in simulation speed. Save All virtually eliminates the need to re-simulate for every debugging task. SILOS III also provides options to save simulation results for pre-selected signals if only a subset of the entire design requires analysis.

Silos Simulation Environment Includes:

The Silos Simulation Environment (SSE) is a set of highly refined multi-tasking utilities developed for the designer to interactively explore, interrogate, analyze and modify Verilog HDL descriptions at the behavioral or gate level. A comprehensive set of interactive graphical tools integrated into SILOS III offers the designer various modes of exploration: viewing and editing of HDL source files, incrementally breakpointing, stepping or timed simulation, real-time viewing of simulation activities, error detection; access and analysis of expressions, variables, modules, signals, vectors and registers.



Silos Simulation Environment Graphical User Interface illustrating the Silos Hierarchy Explorer, Two-Dimensional Signal Tracing Utility and the Silos Data Analyzer.

High Performance Throughput Simulator

SILOS III provides compiled-like simulator performance from an interpreted simulation environment. This means the throughput performance benefits for model development and debugging capabilities without the long compile times inherent with compiled simulators.

Simulation Project Management

SILOS III incorporates a Project Management utility that organizes and saves the numerous files that compose the target simulation run. Project Management will save valuable time in collecting and prioritizing libraries, source code file, stimulus and other related files that must be coordinated with each simulation. It provides for fast save and restarts as well as restoration of a simulation run.

Silos Data Analyzer

The Silos Data Analyzer provides an interactive graphical waveform display. Using the compact random access file produced by the Save All utility, the Analyzer provides a visual model of the simulation results. This powerful graphical tool allows the user to customize the display to their specific requirements. The Silos Data Analyzer has controls for pan and zoom, time1 and time2 timing markers and related timing information window.

Interactive "drag & drop" enables rapid capture and display of any signal or expression and automated utilities allow for signal selection, time- scale, bus radix, status windows, timing markers and bookmarks. User defined buses can be created and displayed on the fly without the need to specify them prior to simulation.

The analyzer can display both digital and analog waveforms produced and saved by the SILOS III simulator.

Two Dimensional Graphical Trace Mode

Trace Input States is a powerful feature which is the centerpiece of SILOS III's unparalleled gate level debugging capabilities. It allows the designer to graphically trace all fan-in connections to any given signal instantly across the entire simulation database. When coupled with the Save-All utility, Trace Input States provides comprehensive tracing of all related connectivity data to a given signal throughout the entire simulation time and the complete circuit topology.

HDL Source Code Editor

The HDL Source Code Editor provides an integrated and interactive window to view and edit the model's Verilog HDL source files. It contains line numbers and indicators for stop, start and breakpoints. Drag & drop enables rapid capture and display of any expression in the Silos Data Analyzer or the Watch Window. The HDL Source Code Editor can be used to observe the real-time execution of the design as well as highlight model specifics.

Hierarchy Explorer

The Silos Hierarchy Explorer is similar in function to Windows NT Explorer and provides a graphical display of the design's hierarchical structure. Drag & drop enables rapid capture, insertion and display of any entity of the hierarchy.

Watch Window

The Watch Window can be used to display the state value for specified variables and expressions while single-stepping the simulation through the design. Variables or expressions can be dragged and dropped into the Watch Window from any HDL source file window, from the Silos Explorer Window, or from the Silos Data Analyzer. The Watch Window also has a control for setting and forcing variables to a value.

Verilog Hardware Description Language

Verilog HDL, IEEE Standard 1364 , is the language of choice for more than 60,000 designers worldwide. It has proven successful in tens of thousands of engineering projects involving every area of electronic design. With more than 200 ASIC and FPGA libraries available, Verilog HDL will continue to be the best HDL for today's and tomorrow's technology.

SILOS III supports the entire Verilog language. Source models are read directly into the parser and checked for semantics, syntax and modeling errors. Switch, gate and behavioral level models written in Verilog HDL are all acceptable, supporting today's top-down design style, where high-level (RTL) models are developed first and then synthesized and optimized to produce incremental detail as the design progresses.

SILOS III supports all Verilog HDL constructs including:

- Specify Blocks
- User Defined Primitives (UDPs)
- Hierarchical Names and Functions
- System Tasks and Compiler Directives
- Standard Delay Format (SDF)
- Programming Language Interface (PLI)

Analog Behavioral Modeling Support (AHDL):

The IEEE is working on extending Verilog HDL's capabilities into the analog domain. With Simucad's vast experience in mixed analog and digital behavioral simulation, SILOS III's developers have carefully extended Verilog HDL to accommodate both integer and floating point I/O pins. Passing numerical values between behavioral modules is particularly useful when modeling analog behaviors such as A/D converters, A/D comparators, phase lock loops, charge pumps, signal noise, etc. To simplify the implementation of analog models, SILOS III's analog extensions support a full range of trigonometric and transcendental functions, e.g., sin, cos, sinh, cosh, exponential and log.

Customer Support

Simucad provides a full range of customer support programs for SILOS III including: product training, an on-line tutorial, telephone support, consultation and custom software development. Simucad also offers an annual software maintenance program which provides exciting new enhancements and features along with the continuing support programs to address your growing simulation requirements.

Exceptional Price Performance

SILOS III is available in a form that best suits your present and future design requirements as well as your budget. It can handle large hierarchical designs on a workstation or a personal computer. SILOS III's features, accuracy and performance make it, by any benchmark standard, the most complete and versatile Verilog HDL-based simulation tool available at any price.

Third Party Interface

SILOS III will function with any third party products that support Verilog HDL.

Hardware Platform Availability

SILOS III is highly portable and runs on a wide range of computers from workstations to personal computers. Please contact Simucad for currently supported platforms.

Platform	*Operating System:*
Pentium PCs	Windows 95
Pentium/Alpha	Windows NT
SUN	Solaris

For More Information and Pricing Please Contact:

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